Examination (SS 2021)

Communication Systems and Protocols

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Exam: Communication Systems and Protocols
Date: July 27, 2021

Participant:
Matr. №:
ID:

Lecture hall:
Seat №:

The following rules apply:

- The writing time of the examination is 120 minutes.
- No examination aids are permitted, except for
  - a DIN-A4 sheet of hand-written notes,
  - a non-programmable calculator, and
  - a dictionary.
- Use only **document-proof writing instruments** and no red ink.
  - Pencils and correction fluid, for example, are not document-proof.
- You are not permitted to use your own writing paper.
- Please do not write on the back sides of the sheets.
- Additional solution sheets are available from the examination supervisors.
  - Make sure that you label all such sheets with your matriculation number.
  - Each additional solution sheet needs to be assigned to exactly one task.

The examination comprises **36 sheets**.

Task	Points	Score
1	32	
2	30	
3	31	
4	30	
5	30	
6	27	
7	31	
8	31	
$\sum$	242	

Task 1: Physical Basics 32

Sampling and A/D conversion

1.1 Name the four classes of signals which exist in communication channels. 4

time-continuous, value-continuous (analog signal)
time-continuous, value-discrete (amplitude quantized signal)
time-discrete, value-continuous (sampled signal)
time-discrete, value-discrete (digital)

Correction hints: *-1pt for each missing/incorrect class; both description and class name are valid*

An exemplary signal is shown below.

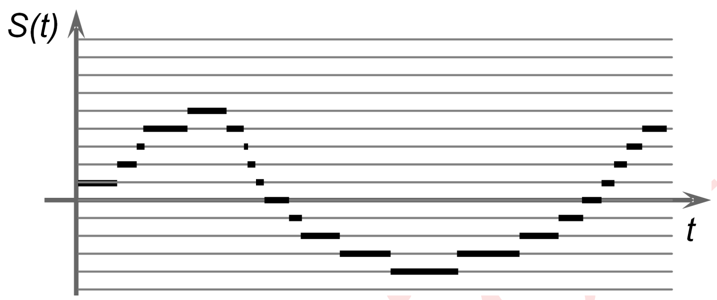


Figure 1.1: Exemplary signal

1.2 Which class does the signal shown in Figure 1.1 belong to? 2

time-continuous, value-discrete / amplitude quantized signal

Correction hints: *2pt if correct*

When integrating an AD converter, a sample & hold gate is needed. An exemplary sample & hold gate is given in Figure 1.2.

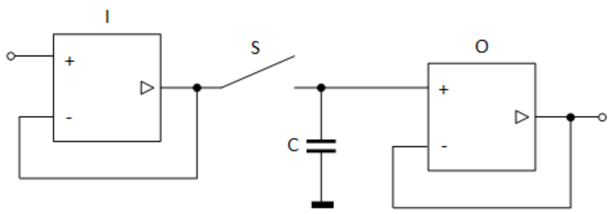


Figure 1.2: Sample & hold gate

1.3 What is the purpose of the sample & hold gate for the AD conversion process? 2

The signal conversion takes time. The signal is not allowed to change during the conversion. Therefore, the value of the input signal has the be kept stable by the sample & hold gate.

Correction hints: *2pt for keeping the signal stable*

1.4 Briefly describe the purpose of every subblock (I, O, S, C) of the sample & hold gate. What is its function inside the sample & hold gate? 8

C The capacitor stores the voltage level of the signal that is to be converted

S Using the switch, the capacitor is loaded up to the value of the signal to be converted

I The impedance converter at the input makes sure that no current is drawn from the input signal that would distort the original value

O The voltage follower avoids a change in the voltage stored on the capacitor if the next stage draws current from the output

Correction hints: *2pt per correct subblock*

Channel capacity

A digital baseband transmission system has a maximum frequency of 30 kHz.

1.5 Assuming an ideal channel, calculate the maximum data rate achievable on this channel using ternary signals? 2

$D_{max} = 2 \cdot f_{limit} \cdot \log_2 V = 2 \cdot 30\,\text{kHz} \cdot \log_2 3 = 95.1\,\text{kbit/sec}$

Correction hints: *1pt for general formula, 1pt for correct value*

1.6 Which problem arises when we keep increasing the number of signal steps in a real channel to achieve a higher data rate? 2

With increasing number of signal steps, the voltage difference between these steps decreases. If this voltage difference is lower than the channel noise level, the noisy signal voltage may reach the voltage of the next higher or lower signal step, leading to an incorrect transmission.

Correction hints: *1pt for noise preventing signal interpretation*
1pt for detailed explanation (noise > distance)

Reflection on wires

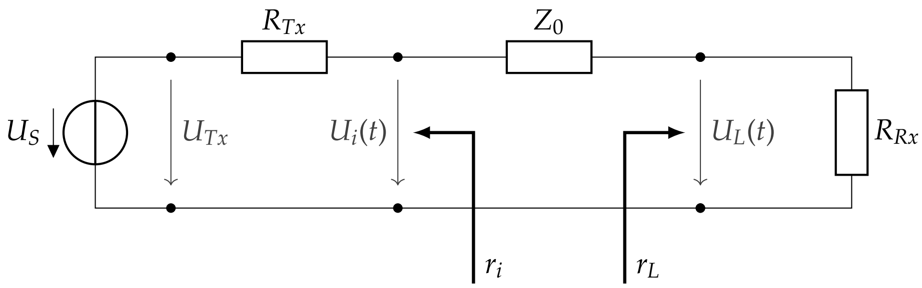


Figure 1.3: Test setup

Figure 1.3 shows the equivalent circuit diagram of an ideal (lossless) transmission line: A transmitter having output impedance R_{Tx} is connected to a receiver with the input impedance R_{Rx} using a long cable.
$R_{Tx} = 60\,\Omega$ and $R_{Rx} = 180\,\Omega$. The signal line is characterized by $Z_0 = 60\,\Omega$.

1.7 Give the generic formula to calculate the reflection factor and give the reflection factors r_i and r_L. 3

$r = (R_T - Z_0)/(R_T + Z_0)$
$r_i = (R_{Tx} - Z_0)/(R_{Tx} + Z_0) = 0$
$r_L = (R_{Rx} - Z_0)/(R_{Rx} + Z_0) = 0.5$

Correction hints: *1pt per correct r_i and r_L value*
1pt for generic formula (or at least one specific form).

At the time $t = 0$ the voltage U_S of the sender changes from 0 V to 5 V and is constant afterwards. The run time of a wave on the cable is t_d.

1.8 Calculate the value of the voltage $U_i(t)$ at the time $t = 0$. 3

At the time $t = 0$ the wave only „sees“ a series connection of the internal resistance R_{Tx} and the wave impedance Z_0.

$$U_i(0) = U_S \cdot \frac{Z_0}{R_{Tx}+Z_0} = 5\,\text{V} \cdot \frac{60\,\Omega}{60\,\Omega+60\,\Omega} = 2.5\,\text{V}$$

Correction hints: *2pt for correct apoproach and formula*
1pt for correct value

1.9 Calculate the voltage $U_m(t)$ in the middle of the line at the times $t \in \{0, t_d, 2t_d, 3t_d\}$. Neglect all transient events, use ideal rectangular impulses for calculation. 6

$U_m(0t_d) = 0\,\text{V}$ (since the wave has not reached this point yet).

$U_m(1t_d) = 2.5\,\text{V}$ (see previous task).

$U_m(2t_d) = U_m(1t_d) + r_L \cdot [U_m(1t_d) - U_{cable,m}(0t_d)] = 3.75\,\text{V}$

$U_m(3t_d) = U_m(2t_d) + r_i \cdot [U_m(2t_d) - U_m(1t_d)] = 3.75\,\text{V}$

In general:

$U_m(t) = U_{cable,m}(t - 1t_d) + r_{i/L} \cdot [U_{cable,m}(t - 1t_d) - U_{cable,m}(t - 2t_d)]$

Correction hints: *For $U_m(0t_d)$ and $U_m(1t_d)$: 1pt per correct value.*
For $U_m(2t_d)$ and $U_m(3t_d)$: 2pt if value is correct, 1pt if value is wrong/missing but formula makes sense.

In case that the idea of monitoring the voltage in the middle of the line was not considered (e.g. $U_m(0) = 2.5\,\text{V}$): No points for $U_m(0)$. Subsequent lines are then graded as described above considering consequential errors.

Task 2: Transmission Principles

30

Line Codes

5

2.1 The value **1101 1001 0101** shall be transmitted through a serial wire communication channel. Complete Figure 2.1 with the digital signals transmitted using each given encoding scheme. All codes start from their lower state (-Level 1 or Level 2).

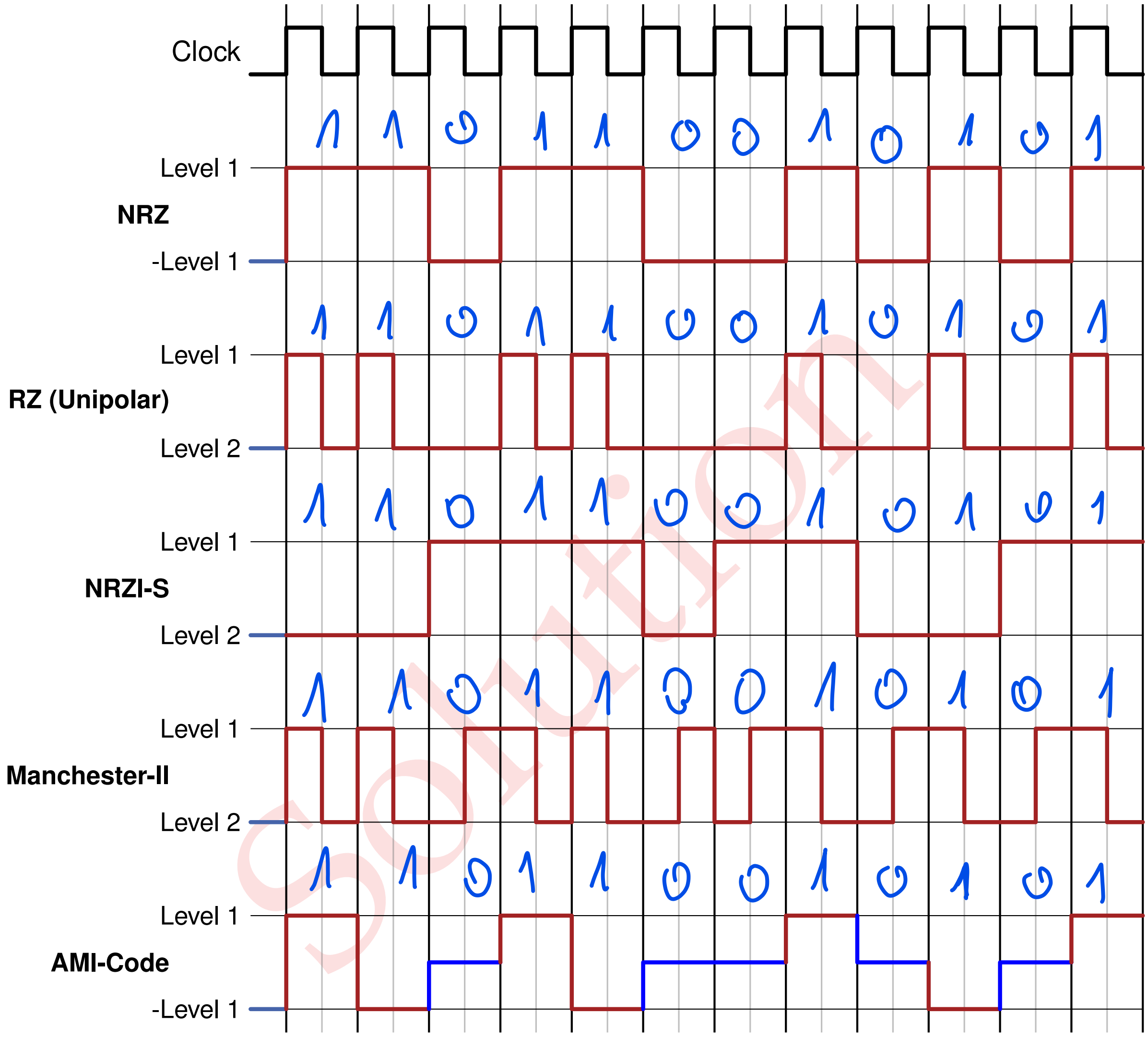


Figure 2.1: Line codes

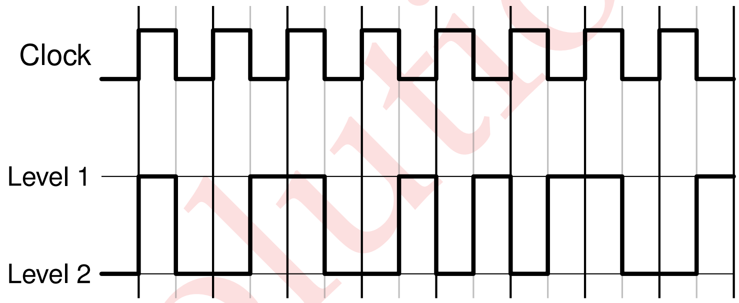
Correction hints: +1 pts. per correct encoding.

2.2 Classify the following line codes according to their clock recovery properties for three possible different inputs, a long sequence of '1's, a long sequence of '0's, and an unknown signal. Mark in the table with a **'yes'** or **'no'** if the code enables the recovery of the clock for the specific input. 4

Input / Code	'1's	'0's	unknown
RZ (Unipolar)	yes	no	no
NRZI-S	no	yes	no
Manchester-II	yes	yes	yes
AMI-Code	yes	no	no

Correction hints: *+1 pts. for each code with all correctly filled columns.*

2.3 What Line code has been used to encode the Data Sequence **1010 0010** below? 3
Under what condition does no DC component exist for the code?
In addition, briefly explain one problem that may arise from a non DC balanced code.



- Manchester-II or Manchester. *AND* Level1 = -Level2, Bipolar
- When transmitting data and power supply voltage over the same line, the supply voltage is affected *OR*
- When using transducers as couplers, varying DC affects data interpretation on receiver's end

Correction hints: *+1 pts. for Line Code and Bipolar condition +2 pts. for explained problem*

Asynchronous Transmissions

2.4 An approach used to synchronize communication processes is Flow Control. Complete the signals in Figure 2.2 to perform two new transmissions with the DATA values 0xA and 0xB using *Level-Triggered Closed-loop Flow Control II*. Ignore delays and consider that: **8**

- the Sender samples and sets signals with the rising edge of CLK_S.
- the Receiver samples and sets signals with the rising edge of CLK_R.
- the Sender and Receiver will set or unset their signals as soon as possible.
- the Receiver requires one clock cycle to consume the incoming data.
- at $t = 0$ ns, BUSY and VALID are '0' and DATA is undefined.

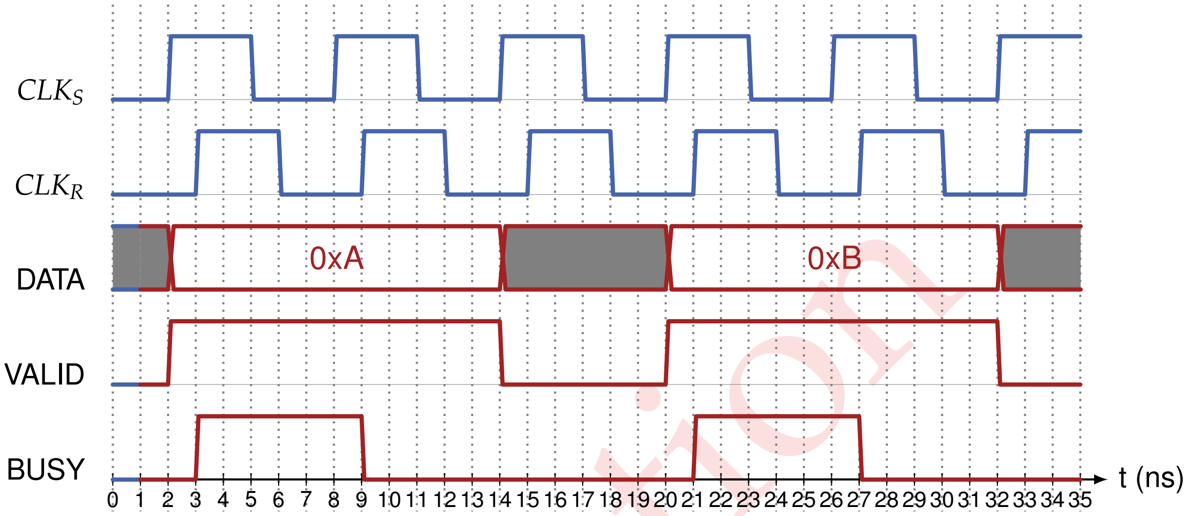


Figure 2.2: Signal sequence

Correction hints: *+4 pts. for correct data and valid transitions +4 pts. for correct busy transitions*

2.5 Give one disadvantage that can occur when using Level-Triggered Closed-Loop Flow Control II? Explain briefly. **2**

- Problems with node synchronization if BUSY signal is asserted too late (data will be removed from the bus too soon)

Correction hints: *+2 pts. if disadvantage correctly explained*

8

2.6 **Start-Stop-mode** is a common synchronisation scheme used in serial asynchronous transmissions. Figure 2.3 presents a serial signal where a value was transmitted using a **7E1** Start-Stop mode (7 data bits, Even parity, 1 Stop bit).
What is the binary value of the data transmitted in this signal? Write it in the space given below. Additionally, identify Start, Stop, Parity, Idle and Data Value fields. Write the name of the fields clearly using the space available in the diagram above the signal. Assume that $CLOCK_R$ is the receiver clock used to sample the incoming signal at the rising edge of the clock.

- 1100101

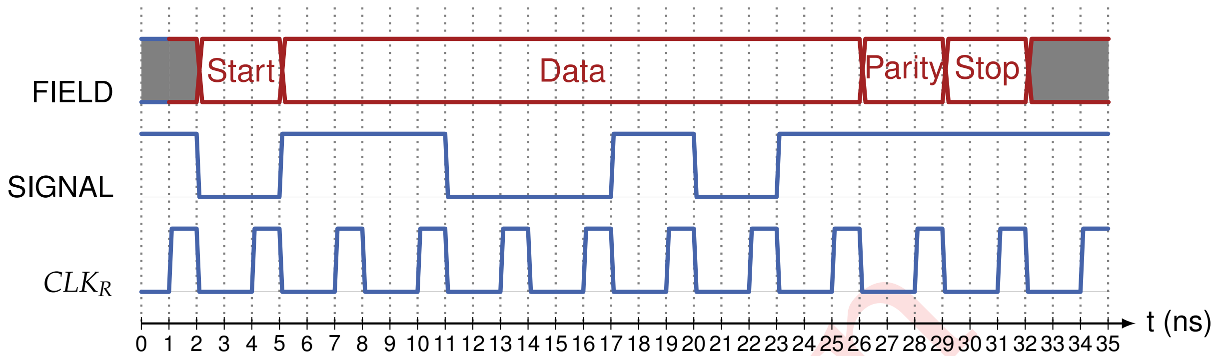


Figure 2.3: Signal sequence with Start-Stop mode

Is the transmitted data error free? Justify your answer.

- Parity bit indicates that an error occured during transmission. (Expected: even parity. Found: odd parity)

Correction hints: *+2 pts. for correct transmitted value*
+1 pts. for each signal part (Start, Data, Parity, Stop, Idle)
+1 pts. for error transmission AND justification

Task 3: Modulation

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Basic Questions

Table 3.1 shows four modulated signals.

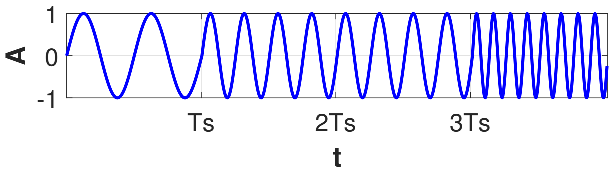
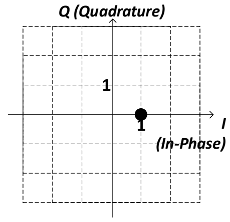
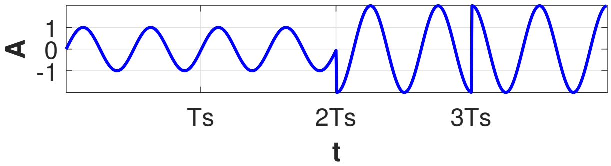
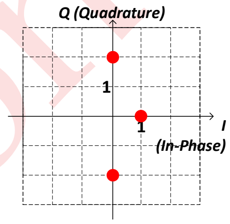
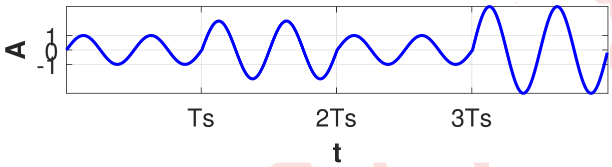
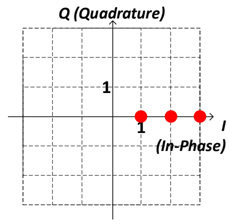
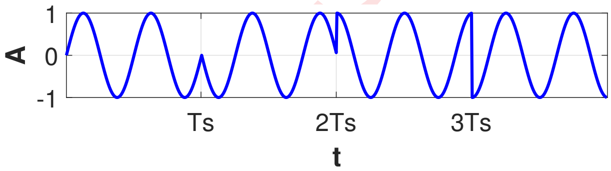
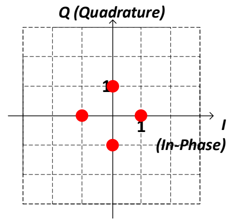
1: Signal	2: Name	3: Constellation Diagram	4: Symbols
	FSK		0,1,1,2
	QAM		0,0,1,2
	ASK		0,1,0,2
	PSK		0,1,2,3

Table 3.1: Modulated signals

3.1 Fill column 2 in Table 3.1 with the modulation names of each modulation. The first row is given as an example. 1

Hint: *Give the most specific modulation, i.e. QAM is only a valid solution if none of the other modulations fit.*

Correction hints:

- *+1 pt. all correct.*

3.2 Fill column 3 in Table 3.1 with the constellation diagram of each modulated signal. The first symbol (leftmost in the waveform) should have phase 0. The first row is given as an example. 6

Hint: *Only add symbols which are actually used in the waveform. Do not include symbols only for symmetry reasons.*

Correction hints:

- *+2 pt. for each diagram.*
- *-1 pt. for each mistake. (no carryover to other diagrams)*

3.3 Fill column 4 in Table 3.1 with the symbols that were modulated in each modulated signal. Assign increasing numbers to symbols in the order as first seen from left to right in the waveform. The first row is given as an example. 3

Correction hints:

- *+1 pt. for each row. Note: Symbols may be doubled, e.g. 0,0; 0,0; 1,1; 2,2;*

Quadrature Amplitude Modulation

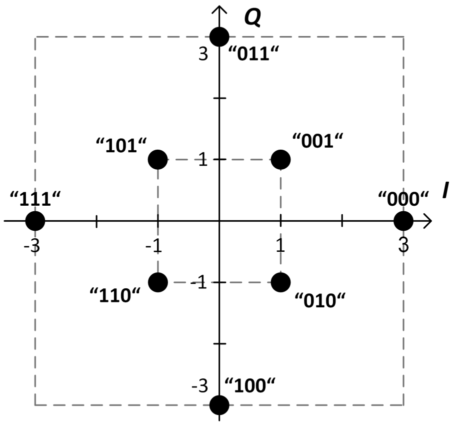


Figure 3.1: QAM constellation diagram

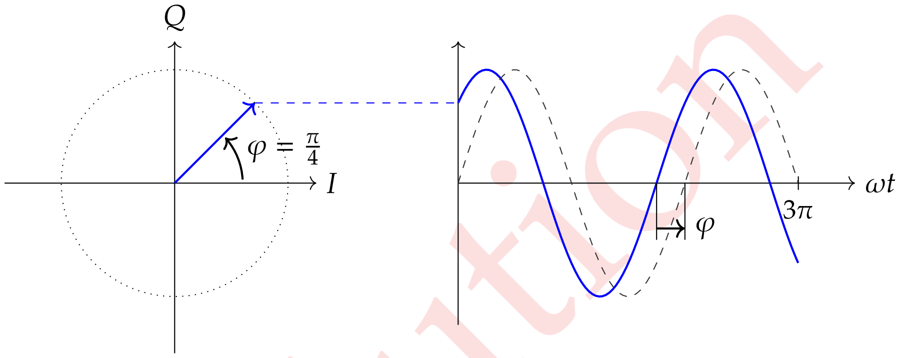


Figure 3.2: Definition of the phase difference of a sine signal compared to a reference signal (dashed line $\widehat{=}$ reference signal).

3.4 The symbol constellation from Figure 3.1 is used by a transmitter to modulate data bits on a carrier. The phase φ of the signal is defined relative to a sine reference signal as shown in Figure 3.2. The modulated signal is shown in Figure 3.3, where Ts is the symbol period. Demodulate the signal and write down the resulting bit-stream. 4

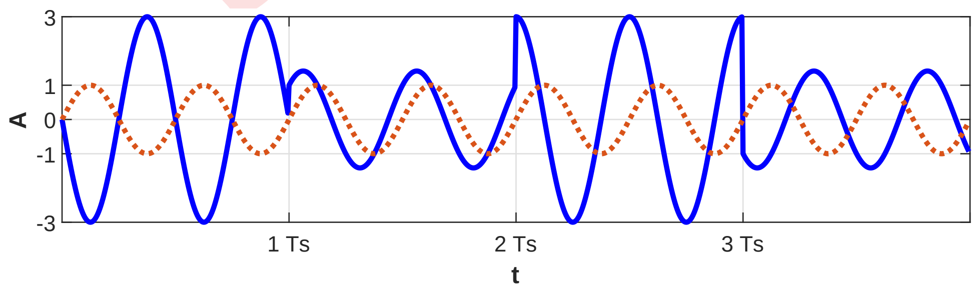


Figure 3.3: QAM modulated signal

Binary Data: 111 001 011 110

Correction hints:

- *+1 pt. per correct symbol.*

3.5 A signal is modulated with the constellation diagram from Figure 3.4 and transmitted on a coaxial cable. The sender is able to generate a maximum voltage amplitude U_{max} of $\pm 10\,V$, the receiver can accept larger voltages. 3

- Calculate the largest possible acceptance radius r_a for the symbols in the constellation diagram, keeping the relative distances between symbols as in Figure 3.4.
- Draw the acceptance radius around each symbol in Figure 3.4.

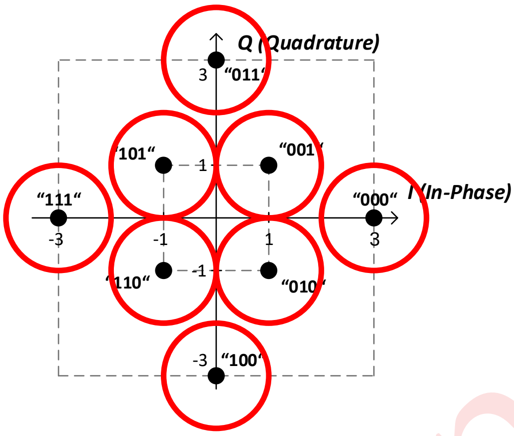


Figure 3.4: QAM constellation diagram: Acceptance radius

The largest amplitude for a symbol to be sent is reached for symbols 011, 000, 100 and 111. Therefore, those symbols can be be at $10\,V$. From the diagrams symmetry, we see:

$$r_a + r_a + r_a = U_{max}$$
$$r_a = \frac{U_{max}}{3}$$
$$r_a = \frac{10\,V}{3}$$

Correction hints:

- *+2 pt. for equation solving.*
- *+1 pt. for drawing the circles.*

3.6 Reconsider the constellation diagram from Figure 3.4. Assume that r_a is $1\,V$, the maximum voltage of the sender is $3\,V$ and the symbols are as given in the figure. Can additional symbols be added without changing any of the previously mentioned parameters? Explain your answer. 2

No: The sender can only generate $3\,V$, so all symbols have to be within a circle with radius 3 around the origin. With r_a of $1\,V$, and keeping the location of existing symbols, it's not possible to put more symbols into the diagram without overlapping acceptance radii.

Correction hints:

- *+2 pt. No with explanation (radii overlap).*

3.7 Explain what the acceptance radius is used for and why it is needed. 1

Real signals are noisy, so the received values will deviate from the exact value in the diagram. The radius determines how much deviation is accepted for a symbol.

Correction hints:

- *+1 pt. real signals are noisy.*

3.8 Assume some data has been transmitted using the constellation diagram from Figure 3.5 on a noisy channel. All received noisy samples have a maximum deviation of amplitude of 1. Depict the noise in Figure 3.5 by drawing at least 5 noisy samples each for the symbols *001* and *100* into the diagram. 2

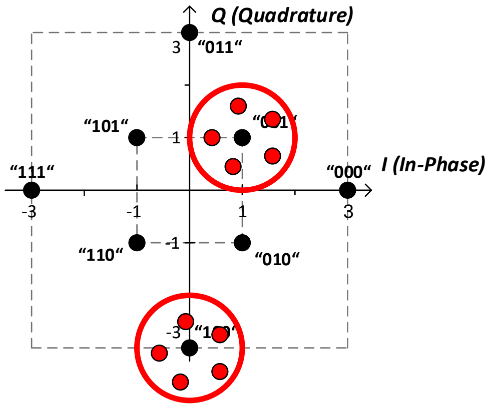


Figure 3.5: QAM constellation diagram: Noise

Correction hints:

- *+1 pt. each symbol. Dots within correct radius 1, circle not needed.*

3.9 If the acceptance radius and location of symbols in the constellation diagram is given, what other aspect related to symbol encoding should be considered to reduce bit errors? 1

Encoding the values to have smaller hamming distance between neighboring values. So a misreceived symbol will lead to less bit errors.

Correction hints:

- *+1 pt. hamming distance.*
- *Accept other sensible solutions.)*

Multiplexing

3.10 What is multiplexing used for? 1

To allow multiple senders to transmit data at the same time.

3.11 Name and shortly explain 2 multiplexing techniques which are not CDMA. 2

TDMA: senders send at different points in time.
FDMA: senders send on different frequencies.

Correction hints:

- *+1 pt. each for name and explanation.*
- *Other sensible solutions must also be accepted (e.g. SDMA).*

Sender Node	Function							
n_0	+1	+1	+1	+1	+1	+1	+1	+1
n_1	+1	-1	+1	-1	+1	-1	+1	-1
n_2	+1	+1	-1	-1	+1	+1	-1	-1

Table 3.2: Walsh functions for nodes

3.12 Table 3.2 shows 3 codes which shall be used for CDMA. What property do these codes have to fulfill to be usable in CDMA schemes? 1

They have to be orthogonal.

3.13 Prove that the codes in Table 3.2 can be used for CDMA. For each individual calculation, provide the approach with variables, **one** step with concrete numbers inserted and the solution. 3

$$n_0 \cdot n_1 = (1,1,1,1,1,1,1,1) \cdot (1,-1,1,-1,1,-1,1,-1) = 0$$
$$n_0 \cdot n_2 = (1,1,1,1,1,1,1,1) \cdot (1,1,-1,-1,1,1,-1,-1) = 0$$
$$n_1 \cdot n_2 = (1,-1,1,-1,1,-1,1,-1) \cdot (1,1,-1,-1,1,1,-1,-1) = 0$$

Correction hints:

- *+1 pt. each for line.*

3.14 Find a fourth Walsh function which is orthogonal to the three Walsh functions in Table 3.3. 1

Sender Node	Function			
n_0	+1	-1	+1	-1
n_1	-1	-1	-1	-1
n_2	+1	-1	-1	+1
n_3	-1	-1	+1	+1

Table 3.3: Only three Walsh functions, but we need four.

Correction hints:

- *+1 pt. for correct solution.*

Task 4: Media Access

30

General questions

4.1 Name two advantages of CSMA/CD in contrast to Aloha. Explain your answers briefly. **2**

Normally no disruption of ongoing transimissions: waiting for free medium
Fast collision detection: Alhoa - collisions can only be identified through a missing acknowledge

Correction hints: *1P for correct advantage (only with explanation)*

4.2 Arrange the media access schemes CSMA/CR, CSMA/CD and Aloha according to their average channel utilization, start with the lowest channel utilization. **1**

Aloha, CSMA/CD, CSMA/CR

Correction hints: *1P for complete correct order*

4.3 CSMA (P-persistent Scheme) is used as transmission scheme. For each transmit request the channel is checked to be free. Briefly describe the behaviour of a node that wants to send data. **2**

The node immediately sends with a probability p, delay transmission for a time span t with a probability 1-p. t is the time for one bit to pass through the communication channel for a node to detect if a second node is trying to send as well

Correction hints: *1p for probability p and sending*
1p for probability (1-p) and wating time span t

4.4 CSMA/CD is used as transmission scheme. Is the length of the media related to the duration of sending? Give a short explanation. **2**

Yes, the data to be send has to be long enough for the signal to travel twice the media during sending time

Correction hints: *1P for correct answer*
1P for travel twice

4.5 How does CSMA/CD react to a collision? Briefly describe the behaviour of a sending node until the message is successfully sent. **2**

sender detects a collision: Transmission of a JAM signal, ceaeses its transmission and waits

Correction hints: *1P for JAM signal*
1P waiting time

Carrier Sense Multiple Access/Collision Resolution

A bus system of four nodes is using CSMA/CR as arbitration scheme and is connected via open collector drivers and a wired-AND connection. Each node has a five Bit identifier and the bus has to cover a maximum distance of 600m.

4.6 Which requirement has to be fulfilled in order to guarantee a faultless function of the system? What are the implications for the transmission rate? 2

The requirement of simultaneity has to be fulfilled.
The signal propagation time t_s is much smaller compared to the digit length (bit time) t_b: $\left[t_s = \frac{l}{v}\right] << \left[t_b = \frac{1}{TR}\right]$.

Correction hints: *1P for Simultaneity*
1P for Transmission rate formula or explanation

4.7 The data format uses a frame with a Start Of Frame bit (SOF) and an identifier with five bits. 4.1 shows an impulse diagram for the bus system described above and the signal level of the shared bus line. Indicate the identifiers of the given nodes as far as possible (use Table 4.1, mark uncertain identifier bits as X). Which node is granted exclusive access to the bus? 6

Node B

node	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4
A	1	0	1	1	X
B	1	0	1	0	0
C	1	1	X	X	X
D	1	0	1	0	1

Table 4.1: Identifiers of the nodes

Correction hints: *1p for each correct address (column) step*
1p for correct winning node
1p if everything is correct

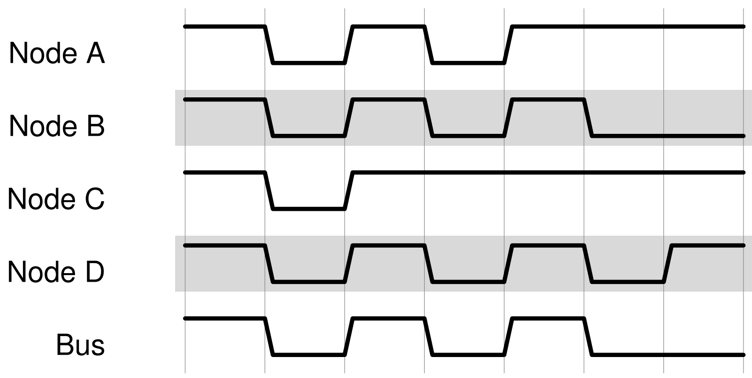


Figure 4.1: Bus Access

Arbitration

4.8 Name one advantage of arbitration compared to static multiplexing schemes like TDMA. Justify your answer briefly. **2**

Dynamic assignment - with static multiplexing an under-utilization off the channel can occur.

Correction hints: *1P for dynamic assignment*
1P for under-utilization

4.9 Explain the differences between centralized and decentralized arbitration schemes briefly. **2**

Centralized: One central arbiter is responsible for the arbitration.
Decentralized: all nodes participate in the selection of the next bus master (there is a rule to select one arbiter)

Correction hints: *1P for one arbiter in centr scheme*
1P for all nodes in decentr scheme or rule for master finding

4.10 Name two benefits of the arbitration scheme Tap Line. Justify your answer briefly. **2**

fair and priority based arbitration possible (priorities can be changed easily)
fast arbitration due to dedicate REQUEST- and GRANT-lines

Correction hints: *1P for each advantage, only with explanation*

7

4.11 A system using Tapline is shown in Figure 4.2. An exemplary arbitration cycle of the system is shown in Figure 4.3. The prioritization is defined as follows: Node 0 > Node 2 > Node 1 > Node 3. The transmission is ongoing and at the time t_0 node 1 and node 2 want to send data. At time t_1 node 3 wants to send data. The sending time for all data packages of all senders are equal. The time steps are shown at the top of the Figure 4.3, complete this diagram accordingly. Mark down the sending nodes and the signal curves of each signal line.

Correction hints: *1P for node3 as first sender*
2p for sequence node2 and node1
2P for correct request removement
1P for correct request at t_1
1P for correct grant C

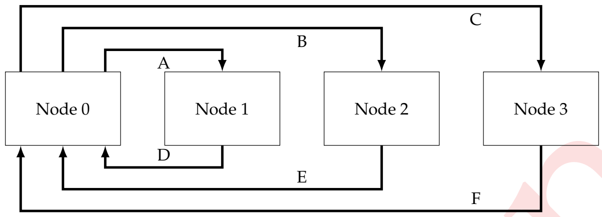


Figure 4.2: Tap Line

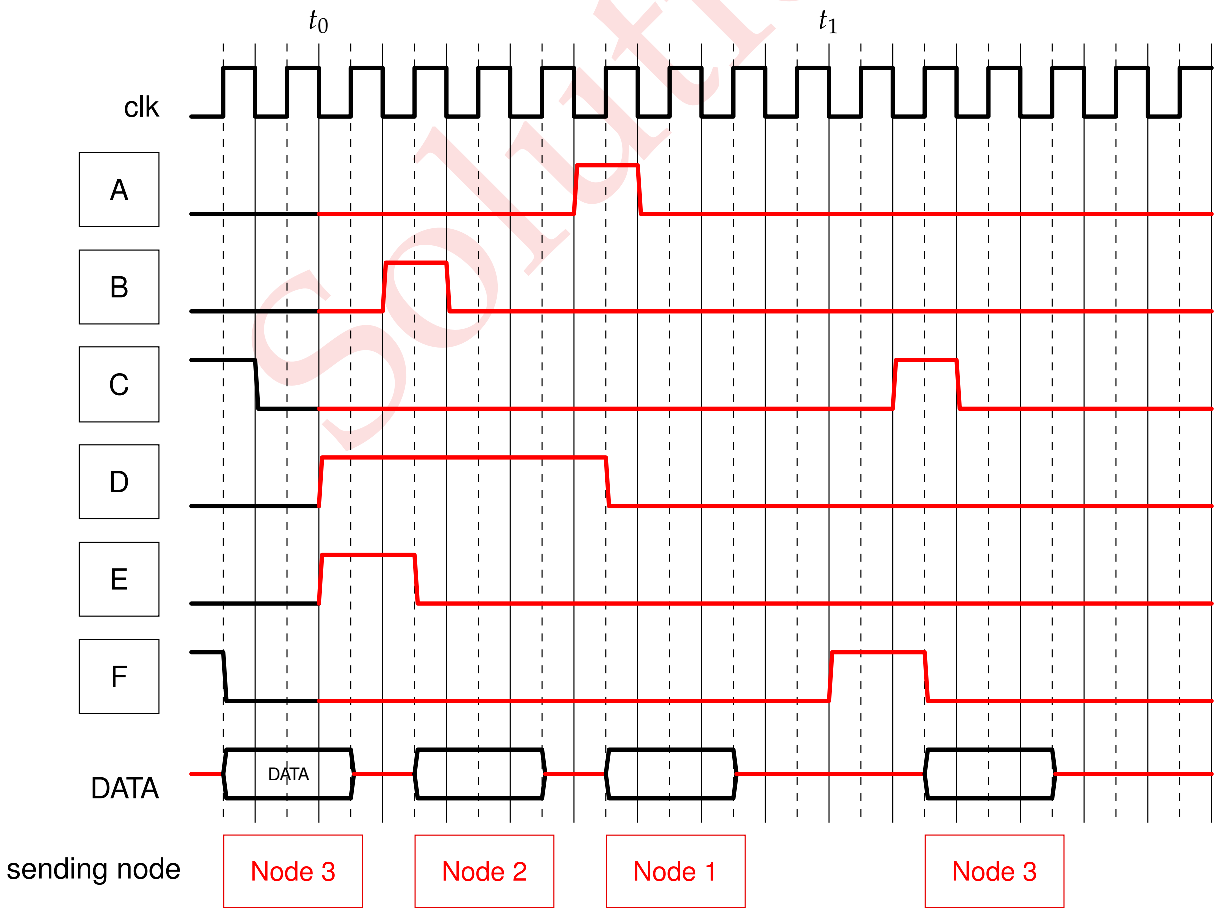


Figure 4.3: Signal flow for Tap Line

Task 5: Error Protection

30

Cyclic Redundancy Check (CRC)

5.1 Does the CRC scheme based on the generator polynomial $G(x) = (x + 1)(x^2 + 1)$ allow a receiver to detect all error patterns with exactly three erroneous bits? Justify. **2**

Yes. Since $(x + 1)$ is a factor of the generator polynomial, every odd number of bit errors is detectable.

Correction hints: *2 pt. for the correct answer.*

5.2 The receiver of a CRC-protected message performs the CRC error detection procedure and calculates a non-zero remainder. What can it reliably conclude with respect to the occurrence of a transmission error? **2**

The receiver can conclude that a transmission error occurred.

Correction hints: *2 pt. for the correct answer.*

5.3 Two nodes use the generator polynomial $G(x) = x^4 + x + 1$ to exchange CRC-protected messages. To transmit a certain message, the sender calculates the corresponding checksum, appends this checksum to the raw message, and finally transmits the bit string **3**

0010 1110 1010 0011.

Due to transmission errors, however, the recipient receives the bit string

0010 1000 0010 0011.

Is the receiver, who is aware of $G(x)$, able to detect this error? Justify your answer based on the error pattern and the specific error detection capabilities of $G(x)$.

Hint: *Do not perform the calculation that the receiver has to perform to detect errors!*

Since the degree of $G(x)$ is 4, all burst errors of length 4 can be detected. The error pattern can be interpreted as a burst error of length 4 and is therefore detectable.

Correction hints:

- *+2 pt. for describing the relevant error detection capability.*
- *+1 pt. for the correct conclusion (only in addition).*

5.4 Given the generator polynomial $G(x) = x^5 + x^4 + 1$, what calculation does the receiver of the CRC-protected bit string "1111 0110 0001" perform as part of its error detection procedure? Give both the dividend and the divisor of this calculation as a bit string. **3**

Hint: *This question does not require you to perform the calculation!*

The receiver calculates the remainder of 1111 0110 0001 : 110001.

Correction hints:

- *+2 pt. for the dividend.*
- *+1 pt. for the divisor.*

5.5 To transmit it over a channel, the message “0100 0111 01” shall be protected by a CRC checksum. Using the generator polynomial $G(x) = x^4 + x^3 + x + 1$, calculate this checksum and give the bit string that is sent to the receiver. 6

```
0 1 0 0   0 1 1 1   0 1 0 0   0 0   :   1 1 0 1 1
  1 1 0   1 1
---------------------------------------------------
  0 1 0   1 0 1
    1 1   0 1 1
---------------------------------------------------
    0 1   1 1 0 1
      1   1 0 1 1
---------------------------------------------------
      0   0 1 1 0   0 1
            1 1 0   1 1
---------------------------------------------------
            0 0 0   1 0 0 0   0
                    1 1 0 1   1
---------------------------------------------------
                    0 1 0 1   1 0
                      1 1 0   1 1
---------------------------------------------------
                      0 1 1   0 1
```

The sender will transmit the bit string “0100 0111 0111 01”.

Correction hints:

- *Starting from 5 pt. for the correct calculation, -3 pt. for not adding the correct number of zeros to the dividend and -2 pt. for every other error.*
- *In addition, +1 pt. for the transmitted bit string.*

5.6 Give the CRC generator polynomial that is implemented by the linear feedback shift register shown in Figure 5.1. 3

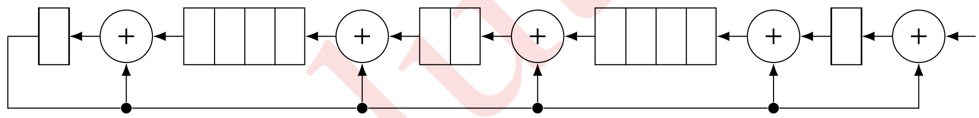


Figure 5.1: Simplified shift register implementation of a CRC scheme

The shift register implements the generator polynomial $G(x) = x^{12} + x^{11} + x^7 + x^5 + x + 1$.

Correction hints: *3 pt. for the correct answer, 1 pt. if there is one mistake.*

Controller Area Network (CAN)

5.7 Consider a CAN network that consists of three individual CAN nodes. One of these nodes, in the following referred to as the sender, transmits a data frame that is received by the remaining two nodes (see Figure 5.3). While the CRC field is transmitted, receiver 1 reads an incorrect value from the bus and, therefore, does not acknowledge the reception of the data frame in the ACK field. Complete the empty columns in Figure 5.3 with the signal values that the three CAN nodes transmit in response to this event and determine the resulting bus level for all columns. 5

***Hint:** Initially, all nodes are in the "error active" state. The general form of a CAN error frame is visualized in Figure 5.2. One column in Figure 5.3 corresponds to one bit duration.*

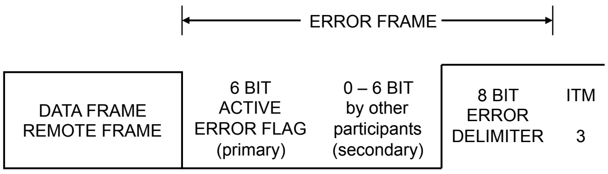


Figure 5.2: Error frame of the CAN protocol

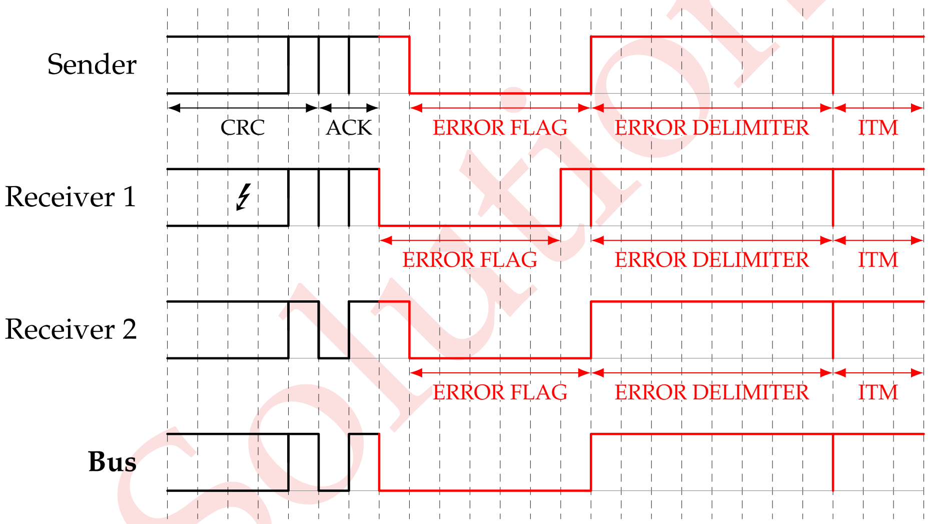


Figure 5.3: Signal sequence diagram of the CAN bus

Correction hints:

- *+1 pt. for each error flag.*
- *+1 pt. for all remaining signal values transmitted by the three nodes.*
- *+1 pt. for the determination of the correct bus level.*

5.8 Explain the bit monitoring rule from the CAN specification and describe how this mechanism is used for the purposes of error detection. 2

During the transmission of a bit, the sending node monitors the bus. If the value on the bus differs from the transmitted value, an error is detected (unless this deviation is explicitly in line with the specification, e.g., for arbitration).

Correction hints: *2 pt. for the correct explanation.*

5.9 Other than the bit monitoring rule mentioned in Task 5.8, name two error detection mechanisms incorporated into the CAN specification. 2

1. Frame format
2. Cyclic redundancy check
3. Acknowledgment mechanism
4. Bit stuffing rule

Correction hints: *+1 pt. per mechanism, no more than 2 pt. in total.*

5.10 How does the error frame transmitted by an "error active" node differ from the error frame transmitted by an "error passive" node? Give a brief explanation. 2

The error frame transmitted by a node that is currently "error active" consists of six consecutive dominant bits, while the error from of an "error passive" node consists of six consecutive recessive bits (unless they are overwritten by dominant bits).

Correction hints: *2 pt. for the correct explanation.*

Task 6: Protocols

27

FireWire Arbitration

The result of the self-identify process for a FireWire network is shown in Figure 6.1. The number shown in the center of each node represents its physical ID given by the self-identify process.

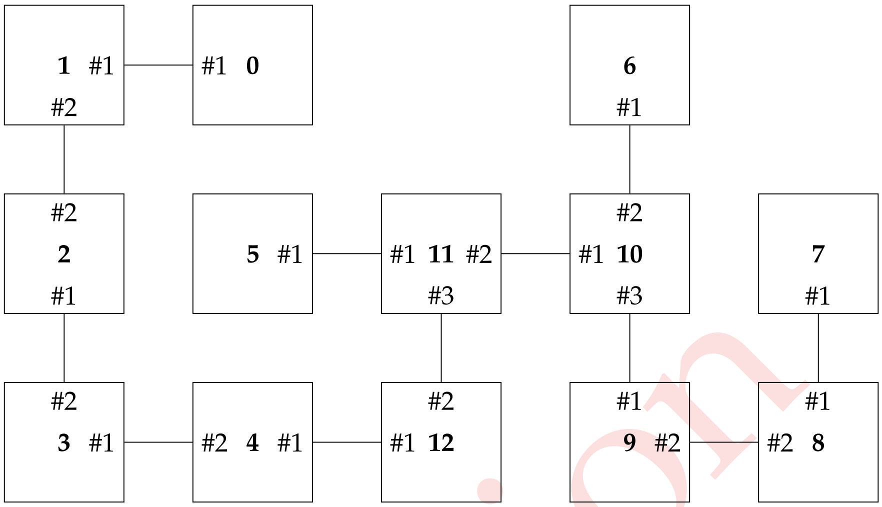


Figure 6.1: FireWire network

6.1 The nodes in Figure 6.1 having address **2**, **5**, **7**, **10** would like to transmit data and start requesting at the same time. Describe in which order are the nodes granted request. 4

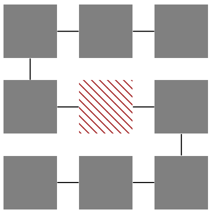
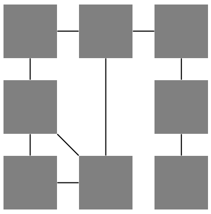
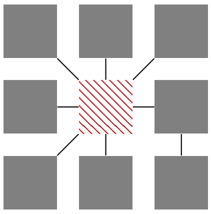
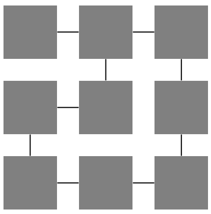
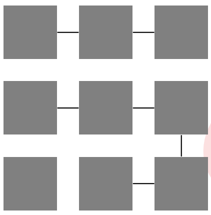
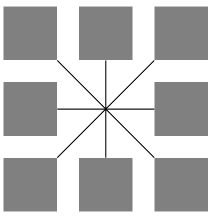
- Assume that every node needs one time unit for processing and forwarding of its request signal.
- If a node receives multiple bus requests, it will always forward the request that it receives from the port with the lowest number.

Granted request order: 5, 10, 2, 7.

Correction hints: *+4 pts. for correct order.*

FireWire Structures

6.2 Different FireWire structures were built, but not all of them are working correctly. State for each row if the nodes shown are building *one connected* FireWire system that is working correctly. If a system is correct, mark its root node. If it is not correct, give a reason for this. 6

	Correct	Wrong	Reason
	x		
		x	Closed loops are unsupported.
	x		
		x	Closed loops are unsupported.
		x	All nodes of one systems have to be connected. Alternate solution: the system is correct, there are three different FireWire systems with the roots marked as being the node at the center of each network
		x	One output cannot have multiple connections.

Correction hints: *+1 pts. per system with reason for wrong cases. Third structure can have two possible roots. The center node or the node to the right of it.*

FireWire Architecture

6.3 Name the three stacked protocol layers of FireWire presented in the lecture. 3

- Transaction layer
- Link layer
- Physical layer

Correction hints: *+1 pts. per layer.*

FireWire Encoding

6.4 Indicate the impulse diagram for the case that the following bit sequence (given in binary notation) should be transmitted: 010110010011_b. Use Figure 6.2. 4

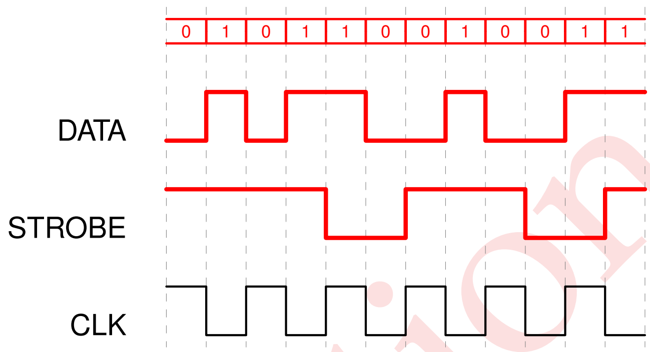


Figure 6.2: FireWire impulse diagram

Correction hints: *+2 pts. for corrent data signal, +2 pts. for correct strobe signal. Inverse of the given STROBE signal is also correct.*

Serial Peripheral Interface Bus (SPI)

The Serial Peripheral Interface bus (SPI) is a synchronous serial communication bus specification used for short distance communication.

The SPI bus specifies the following logic signals:

- **SCLK**: Serial Clock (output from master).
- **MOSI**: Master Output Slave Input (data output from master).
- **MISO**: Master Input Slave Output (data output from slave).
- **SS**: Slave Select (active low, output from master).

Consider the following protocol options and hints:

- The master selects each slave device with a logic level 0 on the individual select line.
- No waiting period between slave select low and first clock cycle.
- No waiting period between slave select high and last data transmission.
- Slave devices have tri-state outputs so their MISO signal becomes high impedance when the device is not selected.
- During each SPI clock cycle, a full duplex data transmission occurs between master and each slave device.

6.5 Draw the timing diagram for the case that the following data byte (given in binary notation) should be transmitted to a single slave: 01101011_b. As part of the transmission, the slave sends back the data byte: 00001101_b.
Assume the data is captured on the rising edge of the clock and all slaves are unselected at the beginning. Use Figure 6.3.

6

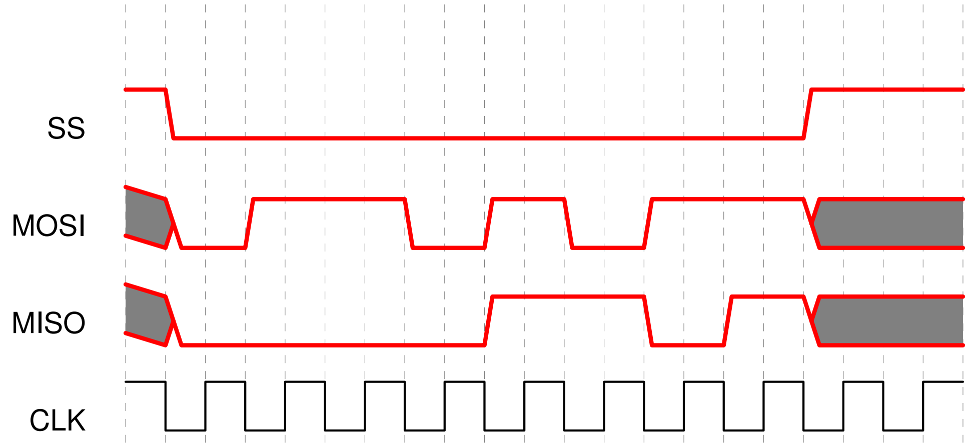


Figure 6.3: SPI full-duplex operation timing diagram

Correction hints: *+2 pts. for corrent SS signal, +2 pts. for correct MOSI signal, +2 pts. for correct MISO signal.*

6.6 Figure 6.4 shows an SPI read operation of **1 byte** from a single slave. Add an appropriate SS signal to the diagram and write down the data the master **reads** from the slave in binary notation.
Assume the data is captured on the rising edge of the clock and all slaves are unselected at the beginning.

4

10010001_b

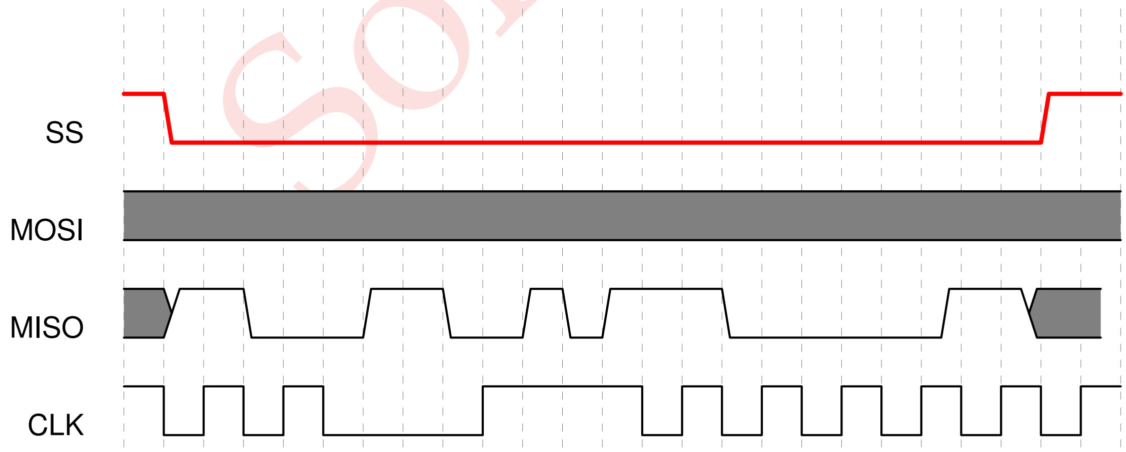


Figure 6.4: SPI read operation timing diagram

Correction hints: *+3 pts. for corrent data, +1 pts. for correct SS signal.*

Task 7: Routing

31

Switching

7.1 The switch matrix crossbars of a router can be implemented using full or reduced crossbars. Describe how both differ in terms of hardware resources and routing capabilities. **2**

reduced crossbar limits concurrent connections,
no limitations on full crossbars,
hardware overhead is smaller for reduced crossbar

Correction hints: *1pt for connection limit, 1pt for hardware overhead. A reasonable answer should give full points.*

7.2 One of the switching modes is *circuit switching*. Explain how the transmission of a message is handled using the different flit types. **3**

Head Flit reserves the path, acknowledgement is sent to sender if path reserved sucessfully,body flits follow the Header flit, tail flit releases the path. Alternate solution: First, a path is established between sender and receiver. The package is then transmitted entirely, afterwards the path is shut down.

Correction hints: *1pt per step (establish path, transmit message, shut down path)*

7.3 Name two advantages and two disadvantages of *circuit switching*. **4**

Advantages: streaming, throughput, simple routers, guarantees (realtime/throughput)
Disadvantages: sporadic transfers, setup required, can block other transmissions

Correction hints: *1pt per advantage and disadvantage*

7.4 Imagine a network with a large link width (e.g. 16 bytes), allowing to fit entire messages within one single flit. Compare this network with another one with smaller link width of one byte. The clock frequency used on both are the same. Most of the messages transferred on both networks are of 10 bytes. Which switching scheme is better suited for which of these networks? Justify your decision. **4**

wide interface packet switching, since circuits would be established for a single flit only

narrow interface circuit switching, as many flits need to be transmitted for a package or message.

Correction hints: *1pt per correct assignment, 1pt per proper reason*

Routing

7.5 Name three optimization goals for a routing algorithm. 3

minimize communication path or time
evenly distribute load over the network
prevent deadlocks
minimize contention
minimize congestion
minimal latencies
short routing path

Correction hints: *1pt each, if more than 3 are given, -1 pt for every wrong answer*

7.6 Explain static and dynamic routing. 2

Static routing predefined/fixed routes computed in advance

Dynamic routing routing info computed during runtime, best path can change

Correction hints: *each reasonable explanation 1pt*

7.7 Figure 7.1 shows a network topology with equal weights w_n on every link. Give the number of hops of the route from node A to F using *minimal routing*. In addition, describe how the number of hops from A to F could change if weights are differing and non-minimal routing is used. 4

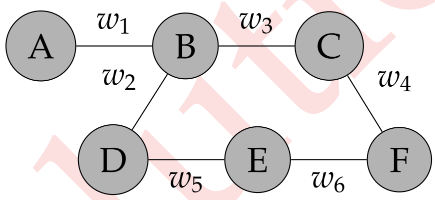


Figure 7.1: A network topology

Hops with minimal routing: 3
If weights are differing, the route using nodes D and E could become the optimal route with 4 hops.

Correction hints: *2pt for 3 hops, 2pt for explanation (node D+E, 4 hops)*

9

7.8 Figure 7.2 represents a network for which an optimal routing has to be found. The weights represent an abstract metric for traffic present at each connection. With node **A** as the starting point, calculate the paths with the lowest total traffic in the network by using Dijkstra's algorithm. Fill in Table 7.1 with the order in which nodes are visited in each step and the shortest paths after visiting the corresponding node.

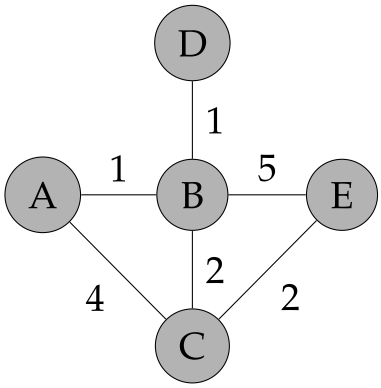


Figure 7.2: Given network topology

	step 0		step 1		step 2		step 3		step 4		step 5	
node	**A**		A		B		D		C		E	
vertex	dist.	pred.	dist.	pred.	dist.	pred.	dist.	pred.	dist.	pred.	dist.	pred.
A	0	A	0	A	0	A	0	A	0	A	0	A
B	∞	-	1	A	1	A	1	A	1	A	1	A
C	∞	-	4	A	3	B	3	B	3	B	3	B
D	∞	-	∞	-	2	B	2	B	2	B	2	B
E	∞	-	∞	-	6	B	6	B	5	C	5	C

Table 7.1: Dijkstra's algorithm

Correction hints: *2 Points steps 1, 2 and 4 each; 1 Point for steps 3 & 5 each; 1 Point for visited nodes*

Task 8: Network-on-Chip

31

General Questions

8.1 Define the edge connectivity of a network. What is the edge connectivity of a 3x7 torus network?

2

Minimum number of edges cut to disconnect a node. 4

Correction hints: *+1 pts. for each correct answer.*

8.2 Name the three basic building blocks in a Network-on-Chip.

3

Network Interface,Routing unit (Router),Link/path

Correction hints: *+1 pts. for each correct answer.*

8.3 Compute the edge connectivity and diameter for the following topologies. All links here are bidirectional. Answer this question by filling in the empty cells in Table 8.1.

8

Topology	Edge Connectivity	Diameter
`6x7 Mesh`	2	11
`7 Node Star`	1	2
`8 Node Ring`	2	4
`3x3x4 Mesh`	3	7

Table 8.1: Topologies and Metrics

Correction hints: *+1 pts. per correct cell.*

8.4 Explain deadlock in a network.

1

A situation where a link is blocked by one transmission that is waiting for the other transmission to finish is called a deadlock./ Mutual blocking of links

Correction hints: *+1 pts. for each correct answer.*

8.5 Name one motivation for using virtual channeles in a NoC router.

1

In larger networks, messages might have to wait for other messages to be transported. Link is blocked for circuit switching. Message buffer is blocked for packet switching To solve this problem of bad link utilization, virtual channels can be used to share the physical link between multiple communications/ Multiplexing of physical links / To avoid deadlocks

Correction hints: *+1 pts. for a sensible answer*

Fault Tolerant Routing

A system which comprises of 25 Processing Tiles is designed. They are interconnected using a NoC and the topology used is a 5x5 mesh. Packet switching is used and XY routing is implemented in the routers.

8.6 Find the path of packets from the source (x,y) = (0,3) to the destination (x,y) = (3,2) using XY routing. In your answer please name all traversed nodes (i.e. their coordinates) in the correct sequence. 3

(0,3) -> (1,3) -> (2,3) -> (3,3) -> (3,2)

Correction hints: *+1 pt. for each correct intermediate node.*

Overtime, certain routers experienced failure. Router at (2,3) stopped working due to internal failure and cannot accept packets anymore. The failed router is illustrated in Figure 8.2. To continue supporting communication between other working routers, XY routing at each router was replaced with a custom adaptive routing algorithm which follows the rules provided below.

Rule1 Try to first route the packet in the X direction towards the destination. Then the Y direction towards the destination. If the link chosen leads to a failed router, do not select this link and go to Rule 2. If the link chosen leads to an already visited router, do not select this link and go to Rule 2.

Rule2 Choose among the remaining directions in the decreasing order of priority +y,-y,+x,-x. Use Figure 8.1 as a guide. If the link chosen leads you to a failed router, do not select this link and repeat Rule 2. If the link chosen leads to an already visited router, do not select this link and repeat Rule 2. If there are no more links available, drop the packet.

8.7 What is the path a packet takes from the source (x,y) = (1,3) to the destination (x,y) = (2,2) using the custom adaptive routing described above? In your answer please name all traversed nodes (i.e. their coordinates) in the correct sequence. Mention which of the above mentioned rules you used to go to the next node. 11

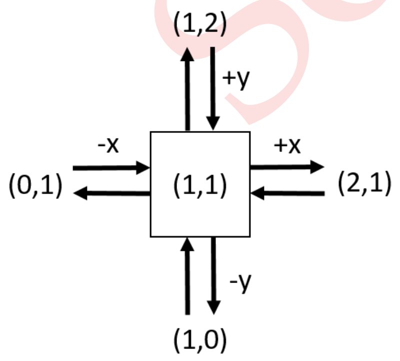


Figure 8.1: Node at (x,y) = (1,1)

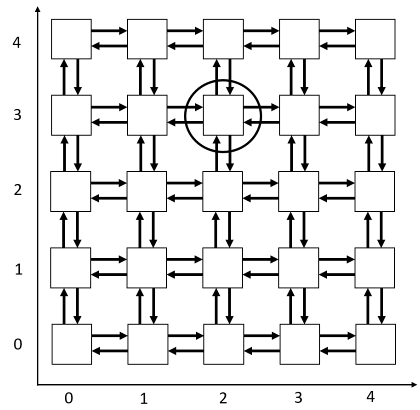


Figure 8.2: 5x5 Mesh network

(1,3) (R2) -> (1,4)(R1) -> (2,4)(R2) -> (3,4)(R2) -> (3,3)(R2) -> (3,2)(R1) -> (2,2)

Correction hints: *+1 pt. per correct intermediate node (start and end node are optional and don't give extra points*
+1 pt. per correct rule mentioned

8.8 Define Minimal Routing. Is the custom adaptive routing used in the previous task minimal? 2

Minimal Routing always chooses the shortest path toward the destination.
No

Correction hints: *+1 pts. for each correct answer.*

Additional sheet for Task ☐: